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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/824,535	04/15/2004	Tomoaki Shino	251996US2	6547

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OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER	
ARENA, ANDREW OWENS	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 07/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/824,535	SHINO, TOMOAKI	
	Examiner	Art Unit	
	Andrew O. Arena	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 April 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4,6,8-10 and 12-17* is/are pending in the application.

4a) Of the above claim(s) *13-17* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4,6,8-10 and 12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5 July 2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites "the area of the body region in contact with the second insulation layer in a cross section along an extending direction of the word line", which is unclear and renders the claim indefinite. The area is a numerical quantity with no direction. Furthermore, the surface measured by said area has a two-dimensional geometry that is not depicted in the claimed cross section. It is unclear what is meant by "the area...in an extending direction".

Claim Objections

Claim 12 is objected to because the recitation "steps on the side surfaces thereof in a cross section along an extending direction of the word line" is somewhat unclear. It may be possible to interpret the extending direction as a limitation only on the cross section, and not the location of the steps.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 4, 6, 8, and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Ohsawa (US 2003/0015757).

Regarding claim 1, Ohsawa discloses (Fig 4A; ¶82) a semiconductor device comprising:

a semiconductor substrate (11);

a first insulation layer (12) formed on the semiconductor substrate;

a semiconductor layer (13+16+17) insulated from the semiconductor substrate by the insulation layer;

a source region (16) of a first conduction type (n) and a drain region (17) of the first conduction type (n) formed in the semiconductor layer;

a body region (13) of a second conduction type (p) formed in the semiconductor layer between the source region and the drain region, said body region being capable of storing data by accumulating or releasing electric charge (col 6 ln 60-61);

a second insulation layer (14) formed on the body region;

a word line (15) formed on the second insulation layer and insulated from the body region by the second insulation layer; and

a bit line (BL) electrically connected to the drain region,

wherein the area of the body region in contact with the first insulation layer is larger than the area of the body region in contact with the second insulation layer in a cross section along an extending direction of the word line (the claimed relationship of areas exists independent of the viewing direction).

Regarding claim 4, Ohsawa discloses (¶86) the first insulation layer has a thickness (30-50nm: ln 7-8) equal to or less than five times the thickness (10nm: ln 2-3) of the second insulation layer.

Regarding claim 6, Ohsawa discloses (¶86) the body region has a thickness (25-50nm: ln 6) equal to or less than three times the thickness (30-50nm: ln 7-8) of the first insulation layer.

Regarding claim 8, Ohsawa discloses (Fig 32; ¶148 ln 1-4) the semiconductor device according to claim 1 further comprising:

a DRAM region including a DRAM having the body region as a part of a memory cell (¶82 ln 1-2);

a peripheral logic circuit (¶148 ln 3) formed around the DRAM region .

Regarding claim 9, Ohsawa discloses a peripheral logic circuit (¶148 ln 3), inherently disclosing a transistor used in the peripheral logic circuit. Ohsawa does not limit his transistor to any particular type, therefore the disclosure of Ohsawa encompasses all well-known transistor types, including those which include:

a source region of the first conduction type and a drain region of the first conduction type both formed in the semiconductor layer;

a body region of the second conduction type formed between the source region and the drain region in the semiconductor layer;

a third insulation layer formed on the body region; and

a gate electrode formed on the third insulation layer and insulated from the body region by the third insulation layer, and

wherein the area of the body region in contact with the first insulation layer is approximately equal to the area thereof in contact with the third insulation layer when viewed in a cross section along the gate electrode.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action (dated 01/25/2006).

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ohsawa as applied to claim 8 above, further in view of Houston (US 6,703,673).

Regarding claim 10, Ohsawa differs from the claimed invention only in not disclosing "the impurity concentration at the interface between the semiconductor substrate and the first insulation layer in the DRAM region is higher than the impurity concentration at the interface between the semiconductor substrate and the first insulation layer in the peripheral logic circuit region."

Houston teaches varying impurity concentration (col 5 ln 35 – col 6 ln 25) in both the DRAM and periphery logic regions independently (col 5 ln 16-17).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made that Ohsawa, in view of Houston, have the impurity concentration at the interface between the semiconductor substrate and the first insulation layer in the DRAM region higher than the impurity concentration at the interface between the semiconductor substrate and the first insulation layer in the peripheral logic circuit region; at least to optimize the transistors independently (Houston: col 5 ln 16-17).

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ohsawa as applied to claim 1 above, further in view of Houston.

Regarding claim 12, Ohsawa differs from the claimed invention only in not disclosing the body region has steps on the side surfaces thereof.

Houston teaches LDD implants (col 6 ln 60), which is known to one of ordinary skill in the art to be effected by source/drain extensions.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Ohsawa in view of Houston by providing source/drain extensions (thus, steps on the side surfaces of the body region in a cross section along an extending direction of the word line); at least to improve transistor performance.

Examiner notes that a cross section along said direction may be taken at the source/body region interface; said cross section would include said steps.

Response to Arguments

Applicant's arguments filed 04/24/2006 have been fully considered but they are not persuasive.

Examiner does not concur that "Ohsawa fails to teach or suggest 'the area of the body region in contact with the first insulation layer is larger than the area of the body region in contact with the second insulation layer in a cross section along an extending direction of the word line' recited in claim 1". As pointed out in the rejection of claim 1 under 35 USC § 112, second paragraph above, the area has no direction. The fact that Ohsawa discloses "the area of the body region in contact with the first insulation layer is larger than the area of the body region in contact with the second insulation layer" remains, regardless of how one chooses to cut and view a cross section of the device.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew O. Arena whose telephone number is (571) 272-5976. The examiner can normally be reached on M-F 8:30-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Andrew O Arena
5 July 2006

Steven Loke
Primary Examiner
Steven Loke